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☐	L4	((detect$3 or determin$3) near4 (frequen$3 near3 (sweep$3 or range$))) same ((pll or ((phase or frequenc$3) near2 lock$3 near2 loop$)))	282
☐	L3	L2 and l1	93
☐	L2	(375/371.ccls. or 375/373.ccls. or 375/374.ccls. or 375/375.ccls. or 375/376.ccls.) or (327/(141-162.ccls.))	181138
☐	L1	((detect$3 or determin$3) near4 (frequen$3 near3 (sweep$3 or range$))) same (pll or ((phase or frequenc$3) near2 lock$3 near2 loop$))	282

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L10: Entry 4 of 70 File: USPT Dec 19, 2000

DOCUMENT-IDENTIFIER: US 6163186 A
TITLE: System including phase lock loop circuit

Application Filing Date (1):
19971110

Current US Class (1):
327

Current US Cross Reference Classification (4):
375/376

Field Of Search Class (1):
327

CLAIMS:

2. A system comprising:

a first switch circuit providing a first voltage;

a second switch circuit providing a second voltage different from the first voltage;

a phase locked loop circuit including:

a phase comparator operated by the first voltage and coupled to receive both a reference clock signal and a feed back clock signal and providing a control signal based on detection of the difference between the reference clock signal and a feedback clock signal;

a charge pump circuit operated by the first voltage and coupled to receive the control signal and providing a control voltage based on the control signal;

a voltage-controlled oscillator operated by the first voltage and coupled to receive the control voltage and providing a clock signal whose frequency is controlled by the control voltage; and

a circuit operated by the second voltage and coupled to receive the clock signal and providing the feedback clock signal; and

a setting circuit coupled to the phase locked loop circuit and detecting whether or not the frequency of the clock signal is in a predetermined frequency range and controlling the phase locked loop circuit so that the phase locked loop circuit provides the clock signal with a frequency placed in the predetermined frequency range when the frequency of the clock signal is detected to be outside of the predetermined frequency range due to the feedback clock signal being electrically disconnected;

wherein the feedback clock signal becomes electrically disconnected in one of the

following three cases including:

a first case in which the second switch does not supply the second voltage to the second circuit;

a second case in which the second circuit does not provide the feedback clock signal even though the second switch supplies the second voltage to the second circuit; and

a third case in which before the feedback clock signal is properly supplied to a phase comparator, the phase comparator outputs a result of a comparison.

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L10: Entry 16 of 70 File: USPT Apr 15, 1997

DOCUMENT-IDENTIFIER: US 5621757 A
TITLE: Circuit for measuring electric field by rapid measurement and normal measurement in a mobile communication system and method of using same

Application Filing Date (1):
19951101

Detailed Description Text (3):
A first local oscillator 120 is provided with a phase-locked loop synthesizer made up of a VCO 121, an amplifier 122, a frequency divider-phase comparator 124, an LPF 125 and a reference signal generator 123 and outputs a local signal S122. The first local oscillator 120 of the present embodiment differs from the first local oscillator 220 of FIG. 1 in that it includes a built-in control-voltage generator 127 and a switching circuit 126. The built-in control-voltage generator 127 generates a control voltage S127 for the VCO 121 such that the frequency of the local signal S122 varies across the entire range of the frequency band for which electric field is to be detected. In the present embodiment, the switching circuit 126 is connected between the frequency divider-phase comparator 124 and LPF 125 of the phase-locked loop synthesizer, and in response to the switching signal S129, connects the frequency divider-phase comparator 124 and LPF 125 and thereby closes the phase-locked loop during normal electric field measurement and, when rapid electric field measurement is required, connects the output S127 of the built-in control-voltage generator 127 to the input of LPF 125. The reason for applying signal S127 by way of LPF 125 to VCO 121 is to prevent erroneous operation due to noise. Accordingly, signal 127 can be applied directly to the VCO 121 as the case demands.

Field of Search SubClasses (1):
224;227;228;344;293;327;376

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L10: Entry 19 of 70 File: USPT Sep 10, 1996

DOCUMENT-IDENTIFIER: US 5555182 A
TITLE: Source quality monitoring system

Application Filing Date (1):
19950504

Brief Summary Text (17):
The transfer function is chosen so that the phase lock loop reacts slowly to changes in the input signals that are being monitored. Slowly reacting phase lock loops generally have a narrow lock range which means the frequency ranges over which they successfully operate are relatively narrow. To force the phase lock loop of the preferred embodiment of the invention to operate over a wider range of frequencies, a frequency detector is added to the phase lock loop. When the frequencies of the source's multi-phase signals and the output from the VCO are different, the frequency detector will drive the phase lock loop in a direction to cause the VCO outputs to match the frequency of the source waveforms.

Field Of Search Class (4):
327

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L10: Entry 28 of 70 File: USPT Apr 19, 1994

DOCUMENT-IDENTIFIER: US 5304955 A

**** See image for Certificate of Correction ****

TITLE: Voltage controlled oscillator operating with digital controlled loads in a phase lock loop

Abstract Text (1):
A phase lock loop operates independent of temperature and process variation by digitally loading a VCO until reaching the desired operating frequency. The VCO reaches a high output frequency even under worst case processing by controlling multiple current mirrors to increase inverter switching current without slowing the response of the VCO to changes in loop node voltage. An Initialize-to-VDD circuit sets the loop node voltage to V.sub.DD so that the load control circuit need only increase loading to slow down the VCO to the desired operating frequency. A frequency range detector monitors the output frequency of the VCO and passes control signals to a load control circuit to activate digital loads and slow down the VCO to the desired operating frequency.

Application Filing Date (1):
19921119

Current US Class (1):
327

First Hit Fwd Refs

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L10: Entry 31 of 70 File: USPT Jan 11, 1994

DOCUMENT-IDENTIFIER: US 5278874 A
TITLE: Phase lock loop frequency correction circuit

Application Filing Date (1):
19920902

Detailed Description Text (3):
The present invention provides a phase lock loop frequency correction circuit. The frequency correction circuit provides a reference frequency which closely approximates a multiple of an unknown frequency of an input signal using both a coarse and fine adjustment operation. The invention locks quickly over a relatively large range of frequencies to provide an output frequency in a timely manner and with a low amount of jitter. Additionally, the coarse adjustment operation allows the invention described herein to detect a range of frequencies of a complex input signal which a voltage controlled oscillator may then use to provide a reference frequency. Therefore, a pre-processing step may be correctly performed to identify the frequency of the input signal with the phase lock loop frequency correction circuit.

Current US Original Classification (1):
375/376

First Hit Fwd Refs

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L10: Entry 34 of 70 File: USPT Dec 22, 1992

DOCUMENT-IDENTIFIER: US 5173927 A
TITLE: Frequency detector system on a digital phase locked loop

Application Filing Date (1):
19901129

Brief Summary Text (7):
The detection system comprises a circuit for synchronizing a digitized input signal (formed from a signal being examined) to a system clock signal, a digital phase locked loop (DPLL) which produces a regenerated digital output signal system from the synchronized digital input signal and a detector circuit which determines if input signal is within a predetermined frequency range. The phase difference sensed by the DPLL between the regenerated digital output and the input signals is linearly dependent on the difference between the frequency of the synchronized input signal and a selectable center frequency of the phase locked loop. The detector circuit detects whether the synchronized signal is within a predetermined detection frequency range. This invention may be applied in the SAT detector of the modem circuit for TACS and AMPS mobile telephones to detect if the SAT signal is being received.

Brief Summary Text (8):
The invention is characterized in that the detector circuit of the frequency detection system comprises a detection timer which forms a detection sequence of the desired length, at the end of which the detection circuitry output signal (SATVAL) is updated. A first phase detector has a first window during which it counts the falling edges of the synchronized input signal (SSAT) coinciding with the window. A second phase detector has a second window during which it counts the falling edges of the synchronized input signal coinciding with the second window. The first and second windows are made up from the regenerated SAT signal (S01) formed by the digital phase locked loop and its 2nd, 4th, and 8th harmonics (S02, S04, S08). If at the end of a detection sequence the counter of the first phase detector exceeds, and the counter of the second phase detector falls short of, their predetermined threshold values, the detector circuit will interpret the frequency of the received signal as correctly falling within the detection frequency range.

Detailed Description Text (4):
The detector circuit 5, a block diagram of which is shown in FIG. 2, is essential for the operation of the present invention. The input signals of the detector circuit are the digital phase locked loop output signals S01, S02, S04, S08 and the received synchronized SAT signal SSAT i.e., to SAT signal, synchronized with the clock signal), as well as the sensitivity selector signal STS and the clock signal, 4.8 MHz. The detector circuit includes a detection timer 6, which forms a detection sequence of the desired length, at the end of which the detector circuit 5 produces an output signal (SATVAL), which is updated as indicated if there has been reception of a SAT signal of the correct frequency. The detector circuit 5 includes two phase detectors VI1 (7) and VI2 (8), based on counters Each of the detectors VI1 and VI2 has its own phase window made up of the signal S01 and its harmonics, obtained from the phase locked loop. The detectors VI1 and VI2 count the falling edges of the input signal SSAT which coincide with the phase window. The windows

are located in such a manner, that, when the phase locked loop 4 is locked within a certain frequency range (called the detection frequency range), within the lock frequency range of the phase locked loop, VI1 is counting continuously and VI2 is not counting.

Detailed Description Text (5):
FIG. 3 illustrates the typical width and location of the phase windows in relation with the incoming and outgoing signals when the phase locked loop 4 is in the locked state. It can be seen that the window of the phase detector VI1 is at the falling edge of the input signal SSAT and the window of VI2 is at the rising edge. Only VI1 is counting, since only the falling edges are counted. Furthermore, in this example VI1 counts only one falling edge per window even if there happen to be more of them, for example because of noise. The detection timer 6 determines the length of the detection sequence, and the counters are always zeroed (i.e., reset) at the beginning of a detection sequence. Whether an incoming signal SSAT is within the detection frequency range can be determined from the final value of the counters at the end of the detection sequence, this is because VI1 ideally counts all the falling edges of the input signals and VI2 does not count a single input signal edge. However, the locations of the edges of an input signal SSAT usually cannot be predicted with such precision because of noise, thus, a threshold value somewhat higher than what the noise would produce is selected for the counter of VI1 and somewhat lower than what the noise would produce for the counter of VI2. If at the end of a detection sequence the counter VI1 exceeds and the counter of VI2 falls short of their respective threshold values, the detector circuit will give a positive result (i.e. that the received signal is really a SAT signal). Both of these conditions must be in force simultaneously. This condition is checked at the AND gate 9.

Detailed Description Text (14):
The detection sequence length has to be selected as a compromise between the detector speed and its noise properties. It is advantageous to select the center frequency of the phase locked loop so that it is the same as the center frequency of the detection frequency range. As seen in FIG. 3 in this embodiment 90.degree. from the falling edge, of the output signal SO1 is selected as the VI1 detection window center point location and 270.degree. from the falling edge of the output signal is selected as the VI2 detection window center point location. The bandwidth of the phase locked loop must be greater than or equal to the width of the detection frequency range. Widening the phase locked loop band speeds up its step response but increases the noise in the output signal. On the other hand, if the bandwidth of the phase locked loop is very close to the width of the detection frequency range, the noise characteristics on the edges of the detection frequency range are clearly poorer than in the middle of the detection band. The detection frequency range width multiplied by two has been found to be a suitable phase locked loop bandwidth in the SAT application. When a suitable phase locked loop bandwidth has been selected, the width of the phase window of VI1 is selected on the basis of the following formula: ##EQU1##

Current US Class (1):
327

Current US Cross Reference Classification (6):
375/373

Current US Cross Reference Classification (7):
375/376

Field of Search SubClasses (2):
316;325;327;341

CLAIMS:

1. A frequency detection system for detecting if an analog input signal frequency is within a predetermined frequency range, comprising:

digitizing means for receiving the analog input signal and converting the analog input signal into a digital input signal;

a synchronization circuit for synchronizing the digital input signal with a system clock signal and producing a synchronized input signal;

a digital phase locked loop having a selectable center frequency and a bandwidth at least as wide as the predetermined frequency range, the phase locked loop receiving the synchronized input signal and producing a digital output signal having 1st, 2nd, 4th, and 8th harmonics, the digital output signal being produced from the synchronized input signal and having a phase determined by a phase difference between the synchronized input signal and the center frequency;

detector circuit means for detecting whether the synchronized input signal has a frequency within the predetermined frequency range, the detector circuit means including:

(a) a timer responsive to the synchronized input signal, the timer establishing a detection sequence having a beginning and an end;

(b) a first phase detector which counts one edge of the synchronized input signal occurring within a first phase window during the detection sequence, the first phase window being formed from the digital output signal of the digital phase locked loop and located to include the occurrence of one edge of an ideal synchronized signal within the predetermined frequency range, the count in said first phase detector being responsive to the beginning of the detection sequence for resetting the count and responsive to the end of the detection sequence for producing a first status signal, the first status signal indicating whether the count of the one edge counted by the first phase detector exceeds a predetermined minimum count; and

(c) a second phase detector which counts the one edge of the synchronized input signal occurring within a second phase window during the detection sequence, the second phase window being formed by the digital output signal of the digital phase locked loop and located to include another edge of an ideal synchronized signal within the predetermined frequency range, the count in said second phase detector being responsive to the beginning of the detection sequence for resetting the count and responsive to the end of the detection sequence for producing a second status signal, the second status signal indicating whether the count of the edges counted by the second phase detector is less than a predetermined maximum count; and

output means responsive to said first and second status signals for forming a signal indicating that the synchronized input signal is within the detection frequency range when the first and second status signals are both received or the synchronized input signal is not within the detection frequency range when either of the status signals is not received.

2. The frequency detection system of claim 1, wherein the phase-locked loop's selectable center frequency is identical to a center frequency of the predetermined frequency range to be detected, the first phase window has a center point located 90.degree. after a falling edge of the digital output signal, and the second phase window has a center point located 270.degree. after the falling edge of the digital output signal.

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L10: Entry 52 of 70 File: USPT Oct 23, 1984

DOCUMENT-IDENTIFIER: US 4479249 A
TITLE: Apparatus for collecting and processing messages transmitted at different signal frequencies

Abstract Text (1):
An apparatus for receiving messages transmitted from a plurality of radio signal sources operating at different frequencies within a predetermined frequency band. Means are provided to frequency scan the receive signals, deriving information for determining the frequency range in which said signals lie. A demodulating phase locked loop is connected to receive the radio frequency signals, and an initial operating frequency for the phase locked loop is provided by the frequency range information determined from the means for frequency scanning. A resetting circuit is included to maintain the phase locked loop oscillator frequency at a value independent of the frequency of the radio signals.

Application Filing Date (1):
19811105

Brief Summary Text (8):
Apparatus is provided which comprises at least one phase locked loop for processing a message which is condition operable condition after determining an range of the frequency of a pure carrier wave preceding the modulated part of the message.

Detailed Description Text (30):
Briefly summarized, synthesizer 326 whose input 327 receives a reference frequency from divider 700 converts the digital indication on its input 324 into an oscillating signal of respective frequency on its output 329, which is passed to a mixer which receives also the output signal of a voltage controlled oscillator 332. The differential signal at the output 334 of mixer 330 is applied to one input of a mixer 336 which receives on its second input the signals on line 249. Ouput 338 of mixer 336 is coupled to a narrow band pass filter 340 having an accurately determined center frequency to apply its resulting output signal on input 342 of a phase comparator 344 receiving on its second input 346 a reference frequency signal out of divider 700. Output 348 of mixer 344 controls via a loop filter 350 the voltage control input of VCO 332 thus completing the phase locked loop 328.